REMARKS

Claims 1-44 are presented for further examination. Claims 1, 2, 6, 13, 14, 17, 18, 23, 25, 29, 31, 32, 35, and 38-41 have been amended. Claims 42-44 are new.

In the Office Action dated January 15, 2003, the Examiner objected to claim 17 and rejected claims 1-37 and 39 under 35 U.S.C. § 112. Applicant will address these issues first.

Claim 17 was objected to as being dependent upon claim 1 which included the objectionable language "before said active area defining step," which the Examiner did not consider to be an actual process step. Applicant has amended claim 1 so that it now recites "a step of forming active areas."

Claim 6 was rejected because the "etching back step" to remove the bird's beak structure was not disclosed in the specification. Applicant directs the Examiner's attention to the specification, page 15, lines 16-22, wherein the step is described. Applicant has amended claim 6 to more clearly recite this step.

The Examiner rejected claims 23-26 because the specification did not describe etching the nitride layer in field regions other than etching "a further deposited nitride layer." Applicant has amended claim 23 to recite the formation of "sinker regions" instead of "field regions." This change has also been made in claim 25. Support for this change is found in the specification at page 21, line 19 through page 22, line 14.

With respect to claim 25, the Examiner stated that it appeared this claim should depend from claim 23 instead of claim 13. However, applicant did intend to have claim 25 depend from claim 13; and hence, the dependency of claim 25 remains unchanged.

All other grounds for objection and rejection under Section 112 have been overcome by the foregoing amendments.

Turning to the merits, claims 1-8, 13, 31, 32, and 36-38 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,599,722 ("Sugisaka et al."). Claims 9, 11, 12, 27-30, 39, and 40 were rejected under 35 U.S.C. § 103(a) as unpatentable over Sugisaka et al. in view of U.S. Patent No. 5,607,875 ("Nishizawa et al."). Claims 14 and 17 were rejected as obvious over Sugisaka et al. in view of U.S. reference 2002/0158270 ("Yamamoto et al."). Claims 15 and 16 were rejected as obvious over Sugisaka et al. in view of U.S. Patent

No. 4,477,310 ("Park et al."). Claims 18, 19, and 21 were rejected as obvious over Sugisaka et al. in view of Wolf. Claims 33-35 and 41 were rejected as obvious over Sugisaka et al. Claims 10, 20, and 22 were objected to but found to be allowable if rewritten into independent form.

Applicant disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

The disclosed and claimed embodiments of the invention will now be described in comparison to the applied references. Of course, the discussion of these embodiments and the differences between the disclosed embodiments and the subject matter described in the applied references does not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

In a first embodiment of the invention, a dielectric trench is formed through use of a hardmask that comprises an oxide layer having a nitride layer formed thereon. The thickness of the nitride layer is such as to guarantee the silicon surface is not etched during the etching step for forming the trench. After forming the trenches, the first nitride layer is removed and a second nitride layer is grown, also on the same oxide as the first nitride layer. This second nitride layer is used for forming local oxide structures (LOCOS) for defining the active area of the components. The LOCOS structure and the relevant process sequence utilize the two distinct nitride layers although these layers are both removed and thus not detectable in the final structure, they are, however, described and well-claimed in the process steps of the first embodiment.

In a second embodiment, the first nitride layer is used as a hardmask for forming the trench and also for forming the LOCOS structure. In this embodiment, the process sequence tends to be simplified for the benefit of a lower cost but to the disadvantage of a minor flexibility in the technology. The nitride layer being residual after the etching of a trench must be of such a thickness as to guarantee the selective formation of the LOCOS structures.

In yet a third embodiment, the single nitride layer is used as a hardmask for forming the trench, whereas the active area is realized without using LOCOS structures since the nitride layer is eliminated before forming the active area itself. In all of the embodiment, the

polysilicon filling in the trench can be doped, both *in situ* and by implant, and the polysilicon filling can be contacted from the surface through surface contacts.

U.S. Patent No. 5,599,722, Sugisaka et al., is directed for forming dielectrically insulated wells without warpage on the SOI substrate. Warping of the wafer is caused by mechanical stress due to the different expansion coefficients associated with the different materials forming the substrate. Sugisaka et al.'s objective is achieved by depositing on the back of the wafer, or by properly not removing the layers that are automatically deposited also on the back during the normal workflow, oxide and polysilicon. Sugisaka et al. teaches the importance of the oxide and polysilicon layers on the back of the wafer to reduce the warpage.

Also, Sugisaka et al. utilizes a sandwich layer as a hardmask for forming a trench. The sandwich layer is made up of a thermal oxide layer (8a), a nitride layer (9), and a deposited oxide layer (10). These are observed in Sugisaka et al.'s Figures 3-5. These layers work as a hardmask during formation of the trench, *i.e.*, during silicon etching of layer 3. This sandwiched hardmask prevents the silicon etching for the trench from also etching the remaining part of the surface. The oxide layer (10) on top of the nitride layer is required because the selectivity of the etching equipment with respect to the silicon does not guarantee a good formation of the trench unless a very thick layer of nitride is used. However, a very thick layer of nitride will cause surface stress and warpage of the wafer, which Sugisaka et al. seeks to avoid. Therefore, Sugisaka et al. utilizes a very thin nitride layer (9) and coats it with a very thick oxide layer (10) that enables better selectivity because the greater thickness oxide layer can be used without creating excessive stress on the silicon surface. This is the reason for the teaching of Sugisaka et al. at column 4, lines 10-14, that the thickness of the oxide film 10 is determined "by means of the etching selection rate of SiO_2 film 10 and silicon substrate 3 such that isolation groove (trench) 12 extends to insulation film 2." Thus, the oxide layer 10 of Sugisaka et al. is absolutely necessary for forming the trench. Without this oxide layer 10, Sugisaka et al.'s purpose would be defeated. Moreover, Sugisaka et al. does not teach the use of two separately-deposited nitride layers as used in the first embodiment of the present invention. Moreover, with respect to the second embodiment of the present invention wherein a single nitride layer is used for realizing

not in claims

both the hardmask for the trench and the LOCOS structure for the active area, adopting Sugisaka et al.'s structure would defeat the purpose of the present invention.

With respect the third embodiment, Sugisaka et al.'s structure cannot be compared because the hardmask and the active areas are realized in completely different ways. Furthermore, Sugisaka et al. does not teach or suggest doping the polysilicon *in situ* in the trench or of realizing a contact structure of the polysilicon.

Nishizawa et al., U.S. Patent No. 5,607,875, relates to the formation of dielectrically-insulated wells formed with an SOI substrate in with a dielectric trench. Nishizawa et al. specifically teaches a hardmask realized with oxide and photoresist, not with nitride. In addition, Nishizawa teaches filling of the trench in a different way than does the present invention. In Nishizawa et al., the filling of the trench is performed with some deposited polysilicon, with the wafer surface during the depositing step being at the crystalline state, whereas the trench walls are oxidized. The deposition of the polysilicon through CVD happens therefore only inside the trench but not on the trench surface because this is undergoing the crystalline step. Therefore, the entire surface is oxidized and the active area is formed. Nishizawa et al.'s objective, however, is of simplifying the process sequence, and this manner of filling the trench simply eliminates the removing step and that of planarizing the surface, which usually occurs in technologies where the trench filling is performed through deposition on the entire surface.

In Yamamoto, the objective relates to the formation of a PNP lateral device with trench formation occurring through a hardmask in oxide and photoresist. Because of the absence of nitride layers for defining the hardmask and the active area and the absence of the SOI substrate, one of ordinary skill would not be motivated to combine the teachings of Yamamoto with that of Sugisaka et al.

Turning to the claims, claim 1 clearly recites an integration process in an SOI substrate that includes at least a dielectrically insulated well. The process comprises an oxidizing step to form an oxide layer, depositing a nitride layer onto the oxide layer, and masking the nitride layer using a resist layer to define openings for forming the at least one dielectric trench. The nitride layer and the oxide layer are etched as masked to form the trench in the substrate, and the

step of oxidizing the sidewalls of the at least one dielectric trench is performed followed by a filling step. As clearly recited in claim 1, the masking step is carried out directly onto the nitride layer. There is no sandwiching of the nitride layer between two oxide layers as taught by Sugisaka et al. Moreover, if one were to apply the teachings of Sugisaka et al. to the present invention, the nitride layer would have another layer, formed of oxide, on the top surface, which would then be masked. Hence, the nitride layer would not be etched and etching of the trench would require at least one additional step. Thus, the present invention provides a more simplified and straightforward manner of forming the trench utilizing only two layers and not three layers. There is absolutely no teaching or suggestion in Sugisaka et al. of eliminating the additional oxide layer (10) to achieve the process of the present invention because doing so would defeat the purpose of Sugisaka et al, which is to avoid warpage of the wafer. Removing the third layer (10) would require increasing the thickness of the nitride to resist subsequent etching, which in turn would cause warping of the wafer. This warping does not occur in the present invention because the etching equipment used for etching is selective enough with respect to the nitride so as not to require sandwich layers of hardmask in oxide as in the Sugisaka et al. disclosure.

Independent claim 38 and independent claim 41 contain limitations similar to that of claim 1. Applicant respectfully submits that claims 1-8, 13, 31, 32, and 36-38 are not anticipated by Sugisaka et al. and claims 33-35 and 41 are not obvious over Sugisaka et al. because there is no teaching or suggestion to one of ordinary skill in this reference that meets all of the limitations of the claimed invention. Moreover, independent claims 39 and 40 recite limitations similar to claim 1 and are also allowable over the Sugisaka et al. reference taken alone or in combination with Nishizawa et al.

For the foregoing reasons, applicant further submits that all claims depending from claim 1 are clearly allowable over Sugisaka et al. taken alone or in combination with Yamamoto et al., Nishizawa et al., Park et al., or Wolf as applied by the Examiner.

In addition, claims 18-22 recite the further step of depositing at least an additional nitride layer and of photomasking and etching the additional nitride layer at locations of field regions. There is no teaching or suggestion in Sugisaka et al., taken alone or in combination with Wolf for achieving the combination recited therein.

New claims 42-44 are allowable claims 10, 20, and 22 rewritten into independent form. More particularly, new claim 42 is dependent claim 10 rewritten to include the limitations of independent claim 1 and intervening claim 9. New claim 43 is allowable claim 20 rewritten to include the limitations of independent claim 1 and intervening 18. New claim 44 is allowable claim 22 rewritten to include the limitations of claim 1 and intervening claims 18 and 21. In view of the finding of allowability of claims 10, 20, and 22, applicant submits that claims 42-44 are now in condition for allowance.

In view of the foregoing, applicant submits all of the claims in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact the applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

Leonardi Salvatore

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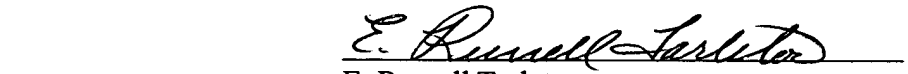

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